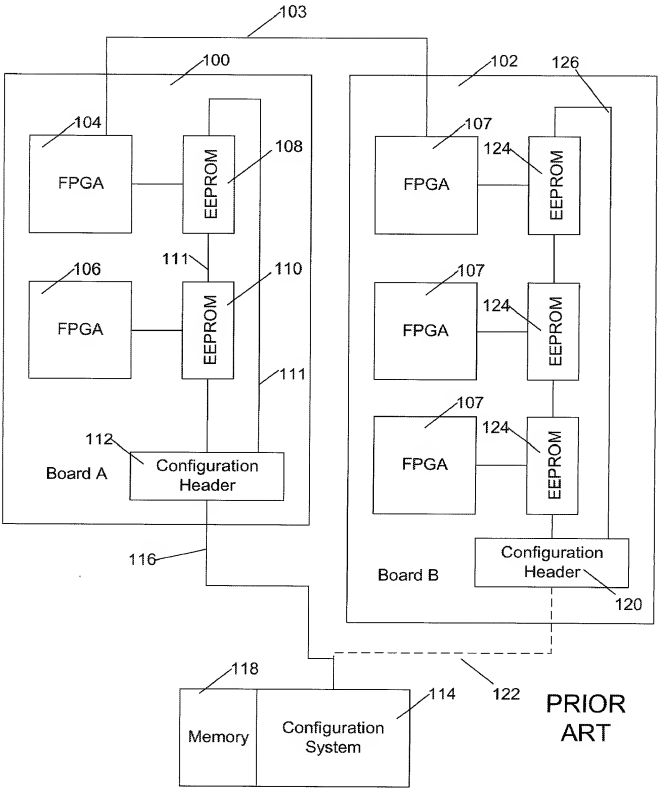

103
100
102
126
104
FPGA
EEPROM
108
107
124
111
106
110
112
Board A
Configuration Header
116
Board B
120
118
Memory
Configuration System
114
122
PRIOR ART

Figure 1

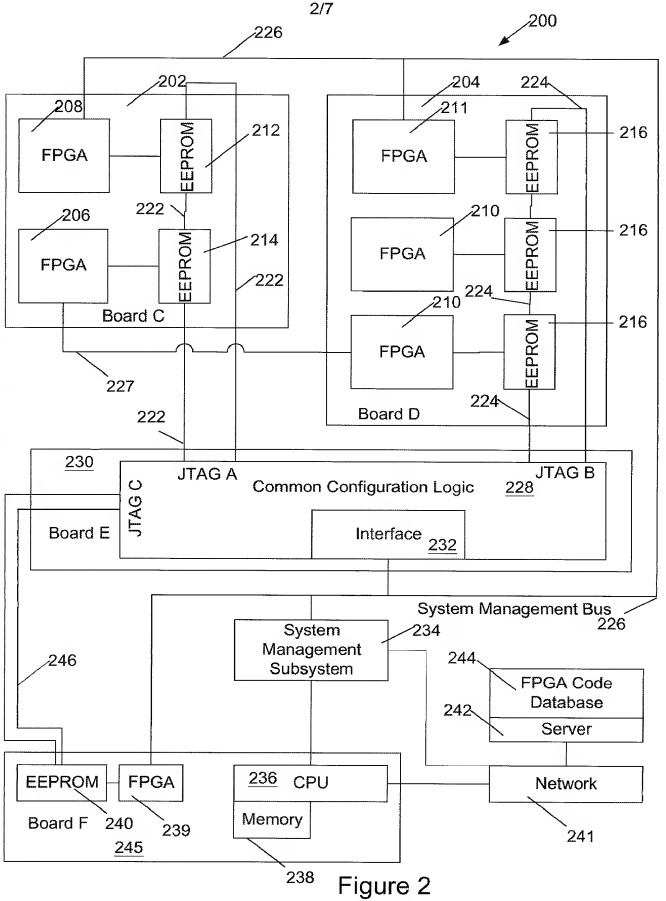

200
226
202
204
224
208
211
FPGA
EEPROM
212
216
222
206
210
214
Board C
227
224
Board D
230
JTAG A
JTAG B
Common Configuration Logic
228
JTAG C
Board E
Interface
232
System Management Bus
226
System Management Subsystem
234
246
244
FPGA Code Database
242
Server
EEPROM
FPGA
236
CPU
Network
Memory
Board F
240
239
241
245
238

Figure 2

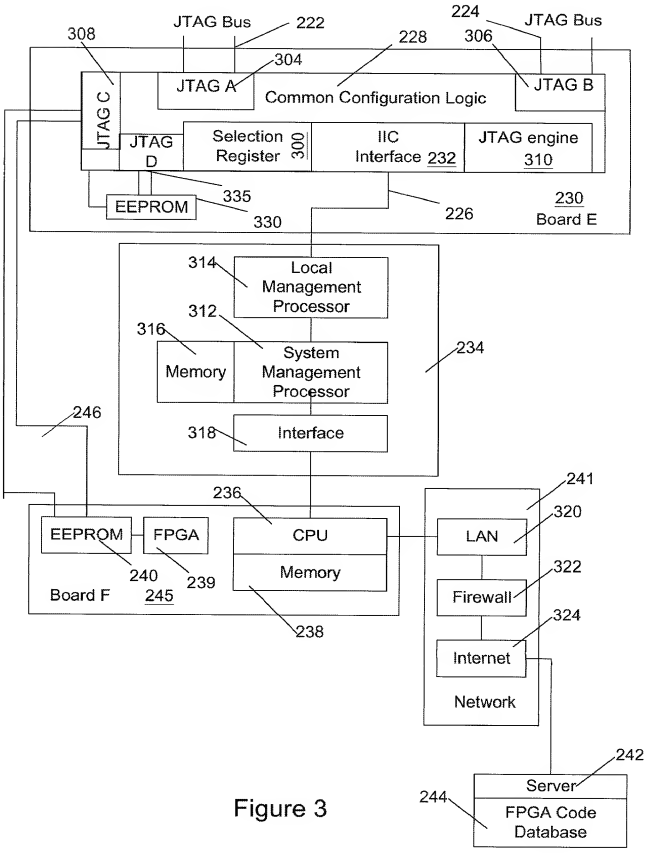

JTAG Bus
222
224
JTAG Bus
308
228
306
304
JTAG A
Common Configuration Logic
JTAG B
JTAG C
JTAG D
Selection Register
300
IIC Interface 232
JTAG engine 310
EEPROM
335
330
226
230
Board E
314
Local Management Processor
312
316
Memory
System Management Processor
234
246
318
Interface
241
236
320
EEPROM
FPGA
CPU
LAN
240
239
Memory
322
Board F
245
Firewall
324
238
Internet
Network
242
Server
244
FPGA Code Database

Figure 3

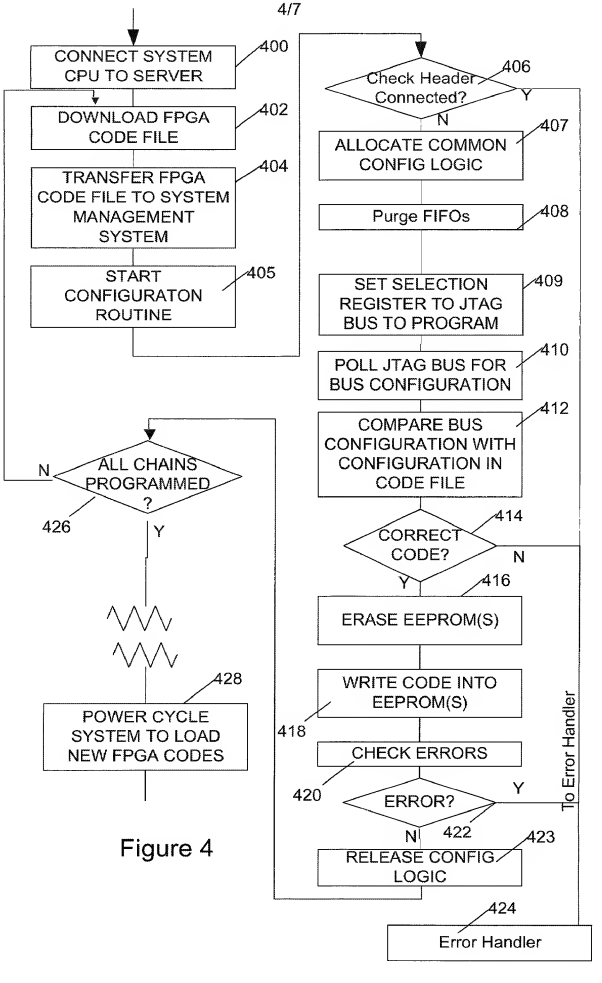

CONNECT SYSTEM CPU TO SERVER
400
DOWNLOAD FPGA CODE FILE
402
TRANSFER FPGA CODE FILE TO SYSTEM MANAGEMENT SYSTEM
404
START CONFIGURATON ROUTINE
405
Check Header Connected?
406
Y
N
ALLOCATE COMMON CONFIG LOGIC
407
Purge FIFOs
408
SET SELECTION REGISTER TO JTAG BUS TO PROGRAM
409
POLL JTAG BUS FOR BUS CONFIGURATION
410
COMPARE BUS CONFIGURATION WITH CONFIGURATION IN CODE FILE
412
CORRECT CODE?
414
N
Y
ERASE EEPROM(S)
416
WRITE CODE INTO EEPROM(S)
418
CHECK ERRORS
420
ERROR?
Y
N
422
RELEASE CONFIG. LOGIC
423
Error Handler
424
To Error Handler
ALL CHAINS PROGRAMMED ?
N
Y
426
POWER CYCLE SYSTEM TO LOAD NEW FPGA CODES
428

Figure 4

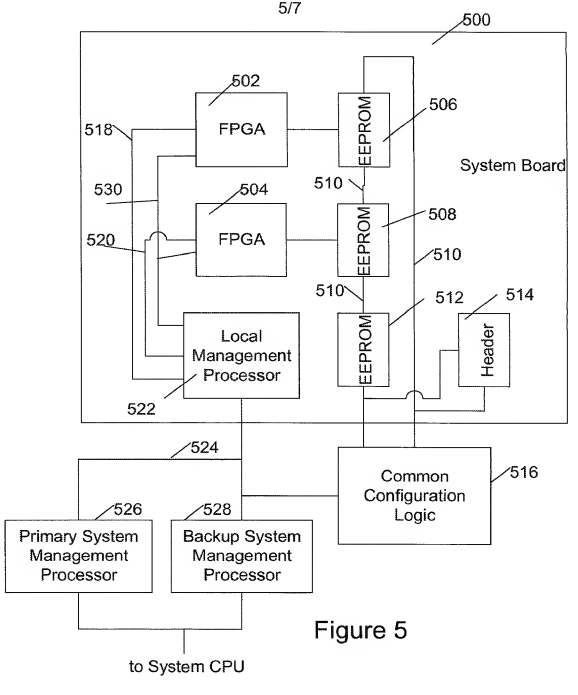


Figure 5

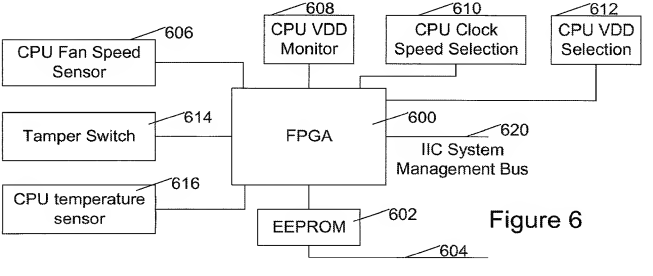
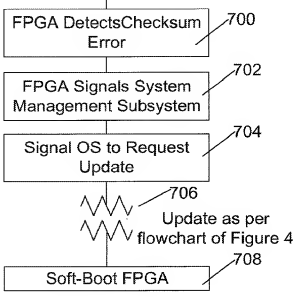


Figure 6

Figure 7



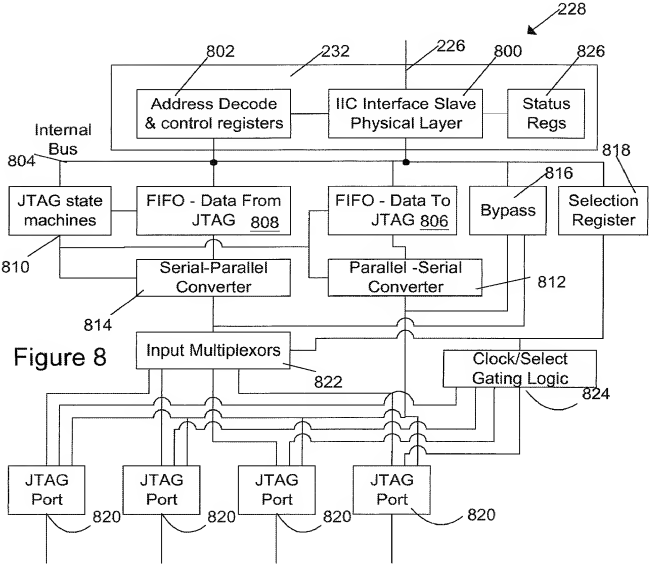


Figure 8

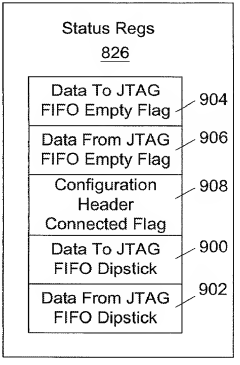

Status Regs
826
Data To JTAG FIFO Empty Flag
904
Data From JTAG FIFO Empty Flag
906
Configuration Header Connected Flag
908
Data To JTAG FIFO Dipstick
900
Data From JTAG FIFO Dipstick
902

Figure 9